Claim Amendments

Claim 1 (currently amended): A switching system comprising:

I input port mechanisms with a width, which receive packets having data from a communication line, where I is greater than or equal to 1 and is an integer;

O output port mechanisms with a width, which send packets to a communication line, where O is greater than or equal to 1 and is an integer;

a carrier mechanism for carrying packets in an allocated time slot, said carrier mechanism having a width wider than the width of the input and output port mechanisms so data from more than one packet at a time is transferred in the allocated time slot, said carrier mechanism connected to each input port mechanism and each output port mechanism;

a memory mechanism in which packets are stored, said memory mechanism connected to the carrier mechanism; and

a mechanism for providing data from more than one packet at a time to the memory mechanism through the carrier mechanism from the input port mechanisms, the

providing mechanism includes input stage queue groups connected to the carrier mechanism and the input port mechanisms for storing packets received by the input port mechanisms, and output stage queue groups connected to the providing mechanism and the output port mechanisms for storing packets to be sent out the output port mechanisms, said providing mechanism transferring more than one packet at a time in the allocated time slot whose total width equals the width of the carrier mechanism in each allocated time slot to the memory mechanism, said providing mechanism transferring more than one packet at a time to the memory mechanism in the allocated time slot only when there is enough data from more than one packet from an input stage queue group to fill the width of the carrier mechanism but not transferring any data from any packets from the input stage queue group in the allocated time slot when there is not enough data to fill the width of the carrier mechanism.

Claim 2 (original): A switching system as described in Claim 1 wherein the width of the carrier mechanism is independent of the width of any packet.

Claim 3 (original): A system as described in Claim 2 wherein the input port mechanism receives variable sized packets.

Claim 4 (original): A switching system as described in Claim 3 wherein the output port mechanism sends variable sized packets to the communication line.

Claim 5 (previously presented): A system as described in Claim 4 wherein the providing mechanism also provides packets from the memory mechanism to the output port mechanisms through the carrier mechanism, said providing mechanism transferring packets or portions of packets whose total data equals the width of the carrier mechanism in each transfer cycle from the memory mechanism.

Claim 6 (canceled)

Claim 7 (previously presented): A system as described in Claim 5 wherein the providing mechanism includes a classifying mechanism which places a packet which is received by the input port mechanism into a corresponding queue group, said classifying mechanism connected to the input port mechanisms and the input stage queue groups.

Claim 8 (original): A system as described in Claim 7 wherein the providing mechanism includes a processing mechanism which places a packet in an output queue group into a corresponding output port mechanism, said processing mechanism connected to the output port mechanisms and the output queue groups.

Claim 9 (original): A system as described in Claim 8 wherein the clarifying mechanism includes a first write finite state machine for writing packets into a corresponding

input queue, the providing mechanism includes a second write finite state machine for writing packets from an input queue group into the memory mechanism, and a first read finite state machine for reading packets from the memory mechanism to an output queue group, and the processing mechanism includes a second read finite state machine for reading a packet from the output queue group to the network.

Claim 10 (original): A system as described in Claim 9 wherein the memory mechanism includes a shared memory.

Claim 11 (original): A system as described in Claim 10 wherein packets or portions of packets travel on the carrier mechanism based on time division multiplexing.

Claim 12 (original): The system as described in Claim 11 wherein the carrier mechanism includes a bus.

Claim 13 (original): A system as described in Claim 12 wherein the first read finite state machine only transfers data of packets of an input queue group to the bus when the input queue group contains at least one cache-line of data.

Claim 14 (original): A system as described in Claim 13 wherein the communication line is an ATM network.

Claim 15 (previously presented): A switching system for packets comprising:

a central resource having a width and an overall bandwidth and input port mechanisms and output port mechanisms each having widths for receiving or sending packets, respectively, said central resource partitioned via time slots that are allocated to the input and output port mechanisms, said central resource width independent of any input or output port mechanisms width and the overall bandwidth can grow without limitation by the input or output port mechanisms width; and

a memory mechanism for storing packets, said memory mechanism connected to the central resource and receiving more than one packet at a time in a respective time slot from the central resource which completely fills the width of the central resource, the central resource transferring more than one packet at a time to the memory mechanism in the respective time slot only when there is enough data from more than one packet to fill the total width but not transferring any data from any packets in the respective time slot when there is not enough data to fill the total width of the carrier mechanism.

Claim 16 (original): A switching system as described in Claim 15 wherein the central resource includes a memory bus.

Claim 17 (original): A switching system as described in Claim 16 wherein the central resource includes queue groups in which packets are classified, and the packets are read from and written into the memory mechanism from the queue groups.

Claim 18 (previously presented): A switching system comprising:

a time division multiplex bus having a width;

a memory mechanism connected to the bus which is accessed via time slots in time division multiplexing of the bus; and

a mechanism for reading and writing data of packets to the memory mechanism through the bus without knowledge of the packet boundaries of the data, the reading and writing mechanism transferring more than one packet at a time to or from the memory mechanism in a respective time slot only when there is enough data from more than one packet to fill the width but not transferring any data from any packets in the respective time slot when there is not enough data to fill the width of the bus.

Claim 19 (currently amended): A switching system comprising:

a time division multiplex carrier mechanism having a width;

a memory mechanism connected to the carrier mechanism which is accessed via time slots in time division multiplexing of the bus; and

an input stage mechanism having a width for providing data of packets to the memory mechanism so the data of the packets fills the width of the bus via time division multiplexing, said bus width being a positive non-integer multiple of the input stage mechanism width a mechanism for providing data of packets having a width to the memory mechanism so the data of the packets fills the width of the bus via time division multiplexing, said bus width a positive non-integer multiple of the packet width greater than one, the input stage mechanism transferring more than one packet at a time to the memory mechanism in a respective time slot only when there is enough data from more than one packet to fill the width but not transferring any data from any packets in the respective time slot when there is not enough data to fill the width of the carrier mechanism.

Claim 20 (previously presented): A method for switching packets having a width comprising the steps of:

receiving a first packet and at least a second packet at a switch mechanism; and

transferring data of the first packet and the second packet to a memory mechanism via time slots in time division multiplexing of a bus having a width only when data from the packets fills a predetermined portion of the width of the bus in a time slot, but not transferring any data from the first and second packets in the time slot when there is not enough data to fill the predetermined portion of the width of the bus, said bus width not a function of the data contained in any packet.

Claim 21 (original): A method as described in Claim 20 wherein the bus width is a positive non-integer multiple of the packet width.

Claim 22 (original): A method as described in Claim 21 wherein the transferring step includes the steps of placing the first packet and at least the second packet in an input queue group; and transferring data in the input queue group during an allocated time slot on the bus to the memory mechanism so the data fills the predetermined portion of the width of the bus.

Claim 23 (original): A method as described in Claim 22 wherein before the transferring data step there is the step of determining that the input queue group has at least

enough data to fill the predetermined portion of the width of the bus before data is transferred to the bus.

Claim 24 (original): A method as described in Claim 23 wherein before the transferring data step there is the step of determining that the input queue group has at least one-cache line of data.

Claim 25 (previously presented): A system as described in Claim 14 wherein the memory mechanism has packets stored in it without knowledge of the packet boundaries of the packets.